4~~3~~. (TWICE AMENDED) The circuit according to claim ~~12~~ 3 [12], wherein said [programmable] logic block [circuit] comprises a product term array.

D1

3~~4~~. (THREE TIMES AMENDED) The circuit according to claim ~~12~~ 1, wherein said programmable logic circuit comprises [a look-up table] one or more logic blocks.

D2

7. (FOUR TIMES AMENDED) The circuit according to claim ~~12~~ 1, wherein said reference clock [frequency] is selected from two or more reference clock signals [frequencies] in response to [(i) a multiplexer and (ii)] a configuration signal.

8. (FOUR TIMES AMENDED) The circuit according to claim 7, wherein said two or more reference clock signals [frequencies] are generated internally to said device.

D3

9. (FOUR TIMES AMENDED) The circuit according to claim 7, wherein said two or more reference clock signals [frequencies] are generated externally to said device.

10. (THREE TIMES AMENDED) The device according to claim ~~12~~ 1, wherein said programmable logic circuit comprises a [A] device selected from a group consisting of programmable logic devices

D4 cont.

D

(PLDs), complex programmable logic devices (CPLDs) and field programmable gate arrays (FPGAs)[, comprising the device of claim 12].

~~11~~ 12. (THREE TIMES AMENDED) A device comprising:

a programmable logic circuit configured to (i) generate one or more control signals and (ii) receive one or more clock signals; and

a phase lock loop circuit configured to generate said one or more clock signals, each capable of oscillating at a different one of a plurality of frequencies, said clock signals generated in response to (i) a reference clock, [and] (ii) said one or more control signals, and (iii) one or more of said clock signals wherein said programmable logic circuit and said phase lock loop circuit are integrated on a single circuit.

~~12~~ 15. (THREE TIMES AMENDED) A method for [providing an integrated] dynamically changing a frequency of operation of a programmable logic circuit [and a phase lock loop circuit] comprising the steps of:

(a) [manipulating information] configuring said programmable logic circuit to generate one or more control signals and receive one or more clock signals; and

(b) generating said one or more clock signals with [said] a phase lock loop circuit , each of said one or more clock signals being:

(i) capable of oscillating at a different one of a plurality of frequencies, and

(ii) generated in response to a reference clock, one or more of said clock signals, [frequency] and said one or more control signals.

---

16 ~~19~~. (THREE TIMES AMENDED) The method according to claim 12 ~~15~~, further comprising the step of:

(c) selecting said reference clock frequency from one or more external clock signals generated externally to said programmable logic circuit.

17 ~~20~~. (THREE TIMES AMENDED) The method according to claim 13 ~~16~~, further comprising the step of:

(d) selecting said reference clock [frequency] from one or more second clock signals generated internally or externally to said programmable logic circuit.

---

18 ~~22~~. (TWICE AMENDED) A device comprising:

means for implementing programmable logic for manipulating information to generate one or more control signals,

wherein said means for implementing programmable logic receives one or more clock signals; and

means for generating said one or more clock signals in response to (i) a reference clock, [and] (ii) said one or more control signals, and (iii) one or more of said clock signals wherein said one or more clock signals are each capable of oscillating at a different one of a plurality of frequencies, said means for implementing programmable logic and said means for generating are integrated on a single circuit.

SUPPORT FOR CLAIM AMENDMENTS

Support for the amendments to the claims may be found in the drawings (e.g., FIGS. 1 and 2) and the specification (e.g., page 6, lines 15-22), as originally filed. As such, no new matter has been added.

R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

The present invention concerns a device comprising a programmable logic circuit and a phase lock loop circuit. The programmable logic circuit may be configured to (i) generate one or more control signals and (ii) receive one or more clock signals. The phase lock loop circuit may be configured to generate the one